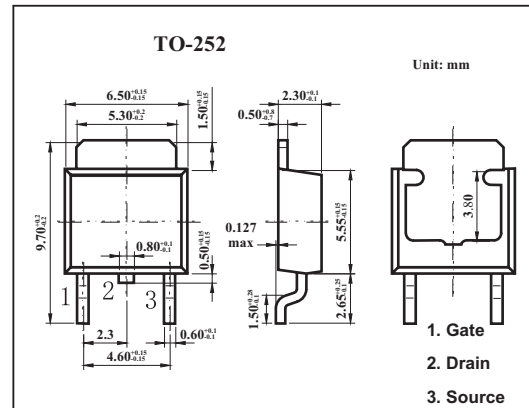
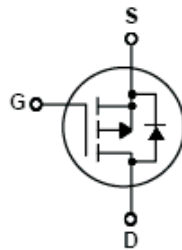


500V P-Channel MOSFET KQD3P50

■ Features

- -1.2A, -500V, $R_{DS(on)} = 4.9 \Omega$ @ $V_{GS} = -10 V$
- Low gate charge (typical 18 nC)
- Low C_{rss} (typical 9.5 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



■ Absolute Maximum Ratings $T_a = 25^\circ C$

Parameter	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	-500	V
Drain Current Continuous ($T_c=25^\circ C$)	I_D	-2.1	A
Drain Current Continuous ($T_c=100^\circ C$)		-1.33	A
Drain Current Pulsed *1	I_{DM}	-8.4	A
Gate-Source Voltage	V_{GSS}	± 30	V
Single Pulsed Avalanche Energy*2	EAS	250	mJ
Avalanche Current *1	IAR	-2.1	A
Repetitive Avalanche Energy *1	EAR	5	mJ
Peak Diode Recovery dv/dt *3	dv/dt	-4.5	V/ns
Power dissipation @ $T_A=25^\circ C$	P_D	2.5	W
Power dissipation @ $T_c=25^\circ C$		50	W
Derate above $25^\circ C$		0.4	W/ $^\circ C$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	$^\circ C$
Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	T_L	300	$^\circ C$
Thermal Resistance Junction to Case	$R_{\theta JC}$	2.5	$^\circ C/W$
Thermal Resistance Junction to Ambient *4	$R_{\theta JA}$	50	$^\circ C/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	110	$^\circ C/W$

*1 Repetitive Rating: Pulse width limited by maximum junction temperature

*2 $I = 102 \text{ mA}$, $I_{AS} = -2.1 \text{ A}$, $V_{DD} = -50 \text{ V}$, $R_G = 25 \Omega$, Startion $T_J = 25^\circ C$

*3 $I_{SD} \leq -2.7 \text{ A}$, $di/dt \leq 200 \text{ A}/\mu\text{S}$, $V_{DD} \leq V_{DSS}$, Startiong $T_J = 25^\circ C$

*4 When mounted on the minimum pad size recommended (PCB Mount)

KQD3P50

■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Testconditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	B _{VDS}	V _{GS} = 0 V, I _D = -250 μ A	-500			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta B_{V_{DS}}}{\Delta T_J}$	I _D = -250 μ A, Referenced to 25°C		0.42		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -500 V, V _{GS} = 0 V			-1	μ A
		V _{DS} = -400 V, T _C = 125°C			-10	μ A
Gate-Body Leakage Current, Forward	I _{GSSF}	V _{GS} = -30 V, V _{DS} = 0 V			-100	nA
Gate-Body Leakage Current, Reverse	I _{GSSR}	V _{GS} = 30 V, V _{DS} = 0 V			100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μ A	-3.0		-5.0	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = -10 V, I _D = -1.05A		3.9	4.9	Ω
Forward Transconductance	g _{FS}	V _{DS} = -50 V, I _D = -1.05A *		2.1		S
Input Capacitance	C _{iss}	V _{DS} = -25 V, V _{GS} = 0 V, f = 1.0 MHz		510	660	pF
Output Capacitance	C _{oss}			70	90	pF
Reverse Transfer Capacitance	C _{rss}			9.5	12	pF
Turn-On Delay Time	t _{d(on)}	V _{DD} = -250 V, I _D = -2.7A, R _G = 25 Ω *		12	35	ns
Turn-On Rise Time	t _r			56	120	ns
Turn-Off Delay Time	t _{d(off)}			35	80	ns
Turn-Off Fall Time	t _f			45	100	ns
Total Gate Charge	Q _g	V _{DS} = -400 V, I _D = -2.7A, V _{GS} = -10 V *		18	23	nC
Gate-Source Charge	Q _{gs}			3.6		nC
Gate-Drain Charge	Q _{gd}			9.2		nC
Maximum Continuous Drain-Source Diode Forward Current	I _S				-2.1	A
Maximum Pulsed Drain-Source Diode Forward Current	I _{SM}				-8.4	A
Drain-Source Diode Forward Voltage	V _{SD}	V _{GS} = 0 V, I _S = -2.1 A			-5.0	V
Diode Reverse Recovery Time	t _{rr}	V _{GS} = 0 V, dI _F /dt = 100 A/μ s, I _S = -2.7A *		200		ns
Diode Reverse Recovery Current	Q _{rr}			1.5		μ C

* Pulse Test: Pulse Width ≤ 300 μ s, Duty Cycle ≤ 2.0%